Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **17EC3046** | **Duration :** | **3hrs** |
| **Sub. Name :** | **HARDWARE DESIGN VERIFICATION TECHNIQUES** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Analyze the importance of functional verification and discuss in detail about the various functional approaches. | CO1 | 12 |
| b. | Develop the design for 4-bit Ripple Carry Adder and also verify the code using test-bench. | CO2 | 8 |
| (OR) | | | | |
| 2. | a. | Describe in detail about the simulation based on clock cycles. | CO3 | 10 |
| b. | You should verify your board design to ensure that the ASICs interoperate properly between themselves and with the third-party components. Complete the verification based on the statement mentioned above. | CO3 | 5 |
| c. | List the need for code reviews? | CO3 | 5 |
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| 3. | a. | Identify the simple concept that would be easy put in practice to overcome the productivity gap in verification. | CO3 | 10 |
| b. | Illustrate the most common verification tools used in conjunction with simulators. | CO3 | 10 |
| (OR) | | | | |
| 4. | a. | Recognize the issue tracking system in which issues are repeatedly reported loud and clear. | CO3 | 10 |
| b. | Recognize a methodology that has been in use in software engineering for quite some time in which the source code is first instrumented. | CO3 | 10 |
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| 5. | a. | Distinguish in detail about different types of coverage that is used by the verification suite. | CO4 | 15 |
| b. | Conclude that the evolutionary system only addresses the lack of owner ship of grapevine system. | CO3 | 5 |
| (OR) | | | | |
| 6. | a. | With neat diagram summarize in detail about levels of verification. | CO4 | 12 |
| b. | The test bench approach requires a similar configuration of the design, use the same abstraction level for the stimulus and response. Determine the appropriate test bench approach. | CO2 | 8 |
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| 7. | a. | Using test vectors, verifying a design is cumbersome and they are hard to interpret and difficult to specify correctly. Find a suitable method for the design to verify it and observing the response. | CO5 | 12 |
| b. | Estimate the first-time success, show how a design is verified, and which test benches are written- Discuss in detail about the verification plan. | CO5 | 8 |
| (OR) | | | | |
| 8. | a. | All design teams have informal systems to track issues and ensure their resolutions.Find the issues and check the functionality of the design. | CO3 | 15 |
| b. | Verify in detail about self checking test benches. | CO5 | 5 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Elaborate about the verification of design using System Verilog. | CO6 | 10 |
| b. | Illustrate in detail about eVC architecture with DUT and eVC. | CO6 | 10 |